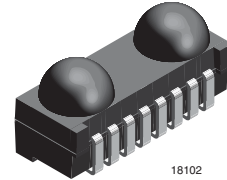


## Serial Infrared Transceiver SIR, 115.2 kbit/s, 2.7 V to 5.5 V Operation

### Description

The TFDU4100 is an infrared transceiver module compliant with the IrDA standard for serial infrared (SIR) data communication, supporting IrDA speeds up to 115.2 kbit/s. The transceiver module consists of a PIN photodiode, an infrared emitter (IRED), and a low-power analog control IC to provide a total front-end solution in a single package. This SIR transceiver is using the small BabyFace package. The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the pulse-width modulation/demodulation function, including Vishay Semiconductors' TOIM4232. At a minimum, a cur-



rent-limiting resistor in series with the infrared emitter and a  $V_{CC}$  bypass capacitor are the only external components required to implement a complete solution.

### Features

- Compliant to the IrDA physical layer specification (Up to 115.2 kbit/s), HP-SIR<sup>®</sup> and TV Remote Control
- 2.7 V to 5.5 V wide operating voltage range
- Low Power Consumption (1.3 mA Supply Current)
- Surface mount package  
- universal (L 9.7 mm × W 4.7 mm × H 4.0 mm)
- Open collector receiver output, with 20 k $\Omega$  internal pull-up.
- BabyFace (Universal) package capable of surface mount solderability to side and to view orientation
- Directly interfaces with various Super I/O and controller devices and Vishay Semiconductors's TOIM4232 I/O
- Built-in EMI protection - no external shielding necessary
- Few external components required
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs, US - Patent No. 6,157,476
- Compliant with IrDA background light specification
- EMI Immunity in GSM Bands > 300 V/m verified
- Lead(Pb)-free device
- Device in accordance to RoHS 2002/95/EC and WEEE 2002/96EC

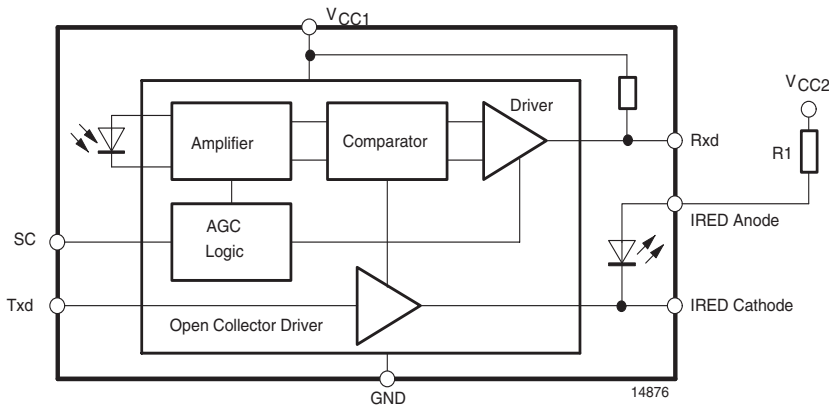
### Applications

- Printers, fax machines, photocopiers, screen projectors
- Telecommunication products (cellular phones, pagers)
- Internet TV boxes, video conferencing systems
- Medical and industrial data collection devices
- External infrared adapters (dongles)
- Data loggers
- GPS
- Kiosks, POS, Point and Pay devices including IrFM - applications

### Parts Table

Part	Description	Qty / Reel
TFDU4100-TR3	Oriented in carrier tape for side view surface mounting	1000 pcs
TFDU4100-TT3	Oriented in carrier tape for top view surface mounting	1000 pcs

## Functional Block Diagram



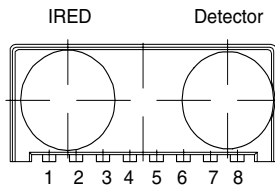
## Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	IRED anode, should be externally connected to VCC2 through a current control resistor		
2	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	Txd	Transmit Data Input	I	HIGH
4	Rxd	Received Data Output, open collector. No external pull-up or pull-down resistor is required (20 kΩ resistor internal to device). Output data is invalid during transmission.	O	LOW
5	NC	No internal connection		
6	V <sub>CC1</sub>	Supply Voltage		
7	SC	Sensitivity control	I	HIGH
8	GND	Ground		

### Pinout

TFDU4100  
weight 200 mg

#### "U" Option BabyFace (Universal)



17087

### Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

### Absolute Maximum Ratings

Reference point Ground (pin 8) unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range	$0\text{ V} \leq V_{CC2} \leq 6\text{ V}$	$V_{CC1}$	- 0.5		+ 6	V
	$0\text{ V} \leq V_{CC1} \leq 6\text{ V}$	$V_{CC2}$	- 0.5		+ 6	V
Input current	for all pins, except IRED anode pin				10	mA
Output sink current					25	mA
Power dissipation	see derating curve	$P_D$			200	mW
Junction temperature		$T_J$			125	°C
Ambient temperature range (operating)		$T_{amb}$	- 25		+ 85	°C
Storage temperature range		$T_{stg}$	- 25		+ 85	°C
Soldering temperature	see recommended solder profile			215	240	°C
Average IRED current		$I_{IRED(DC)}$			100	mA
Repetitive pulsed IRED current	$t < 90\text{ }\mu\text{s}$ , $t_{on} < 20\%$	$I_{IRED(RP)}$			500	mA
IRED anode voltage		$V_{IRED(A)}$	- 0.5		+ 6	V
Transmitter data input voltage		$V_{TxD}$	- 0.5		$V_{CC1} + 0.5$	V
Receiver data output voltage		$V_{RxD}$	- 0.5		$V_{CC1} + 0.5$	V

### Eye safety information

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Virtual source size	Method: (1-1/e) encircled energy	d	2.5	2.8		mm
Maximum intensity for class 1	IEC60825-1 or EN60825-1, edition Jan. 2001	$I_e$			*) (500)**)	mW/sr

\*) The device is a "class 1" device.

\*\*\*) IrDA specifies the max. intensity with 500 mW/sr.

### Electrical Characteristics

#### Transceiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supported data rates	base band		2.4		115.2	kbit/s
Supply voltage	receive mode	$V_{CC1}$	2.7		5.5	V
	transmit mode, $R2 = 47\ \Omega$ (see recommended application circuit)	$V_{CC2}$	2.0		5.5	V
Supply current pin $V_{CC1}$ (receive mode)	$V_{CC1} = 5.5\text{ V}$	$I_{CC1(Rx)}$		1.3	2.5	mA
	$V_{CC1} = 2.7\text{ V}$	$I_{CC1(Rx)}$		1.0	1.5	mA
Supply current pin $V_{CC1}$ (avg) (transmit mode), 20% duty cycle	$I_{IRED} = 210\text{ mA}$ (at IRED anode pin), $V_{CC1} = 5.5\text{ V}$	$I_{CC1(Tx)}$		5.0	5.5	mA
	$I_{IRED} = 210\text{ mA}$ (at IRED anode pin), $V_{CC1} = 2.7\text{ V}$	$I_{CC1(Tx)}$		3.5	4.5	mA
Leakage current of IR emitter, IRED anode pin	$V_{CC1} = \text{OFF}$ , $TxD = \text{LOW}$ , $V_{CC2} = 6\text{ V}$ , $T = -25\text{ to }+85\text{ }^{\circ}\text{C}$	$I_{L(IREDA)}$		0.005	0.5	$\mu\text{A}$
Transceiver power on settling time		$T_{PON}$			50	$\mu\text{s}$

### Optoelectronic Characteristics

#### Receiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance	$\text{BER} < 10^{-8}$ (IrDA specification)					
	$\alpha = \pm 15\text{ }^{\circ}$ , $\text{SC} = \text{LOW}$ , $\text{SIR}$	$E_e$		20	35	$\text{mW}/\text{m}^2$
	$\alpha = \pm 15\text{ }^{\circ}$ , $\text{SC} = \text{HIGH}$ , $\text{SIR}$	$E_e$	6	10	15	$\text{mW}/\text{m}^2$
Maximum detection threshold irradiance	$\alpha = \pm 90\text{ }^{\circ}$ , $V_{CC1} = 5.0\text{ V}$	$E_e$	3.3	5		$\text{kW}/\text{m}^2$
	$\alpha = \pm 90\text{ }^{\circ}$ , $V_{CC1} = 3.0\text{ V}$	$E_e$	8	15		$\text{kW}/\text{m}^2$
Logic LOW receiver input irradiance	Note: No detection below this input irradiance	$E_e$	4			$\text{mW}/\text{m}^2$
Output voltage - Rxd	Active, $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$	$V_{OL}$		0.5	0.8	V
	non-active, $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$	$V_{OH}$	$V_{CC1} - 0.5$			V
Output current - Rxd	$V_{OL} < 0.8\text{ V}$	$I_{OL}$		4		mA
Rise time - Rxd	active to inactive $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$ to $V_{CC1}$	$t_{r(Rxd)}$	20		200	$\mu\text{s}$
	active to inactive $C = 15\text{ pF}$ , internal load only	$t_{r(Rxd)}$	20		1400	$\mu\text{s}$



Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Fall time - Rxd	active to inactive C = 15 pF, R = 2.2 k $\Omega$ to V <sub>CC1</sub>	t <sub>r(Rxd)</sub>	20		200	$\mu$ s
	active to inactive C = 15 pF, internal load only	t <sub>r(Rxd)</sub>	20		200	$\mu$ s
Pulse width - Rxd output		t <sub>PW</sub>	1.63	4	4.3	$\mu$ s
Jitter, leading edge of output signal	over a period of 10 bit, 115.2 kbit/s	t <sub>j</sub>			2	$\mu$ s
Latency		t <sub>L</sub>		100	500	$\mu$ s

### Transmitter

T<sub>amb</sub> = 25 °C, V<sub>CC</sub> = 2.7 V to 5.5 V unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current	IRED operating current can be adjusted by variation of R1. Current limiting resistor is in series to IRED: R1 = 14 $\Omega$ , V <sub>CC2</sub> = 5.0 V	I <sub>d</sub>		0.2	0.28	A
Logic LOW transmitter input voltage		V <sub>IL(Txd)</sub>	0		0.8	V
Logic HIGH transmitter input voltage		V <sub>IH(Txd)</sub>	2.4		V <sub>CC1</sub> + 0.5	V
Output radiant intensity	In agreement with IEC825 eye safety limit, if current limiting resistor is in series to IRED: R1 = 14 $\Omega$ , V <sub>CC2</sub> = 5.0 V, $\alpha = \pm 15^\circ$	I <sub>e</sub>	45	140	200	mW/sr
	Txd logic LOW level	I <sub>e</sub>			0.04	mW/sr
Angle of half intensity		$\alpha$		$\pm 24$		$^\circ$
Peak wavelength of emission		$\lambda_p$	880		900	nm
Half-width of emission spectrum				45		nm
Optical rise time, fall time		t <sub>ropt</sub> , t <sub>fopt</sub>		200	600	ns
Optical overshoot					25	%
Rising edge peak-to-peak jitter of optical output pulse	Over a period of 10 bits, independent of information content	t <sub>j</sub>			0.2	$\mu$ s

## Recommended Circuit Diagram

The only required components for designing an IrDA® compatible application using Vishay Semiconductors SIR transceivers are a current limiting resistor to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure 1). It is recommended that the capacitors C1 and C2 are positioned as near as possible to the transceiver power supply pins. A tantalum capacitor should be used for C1, while a ceramic capacitor should be used for C2 to suppress RF noise. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

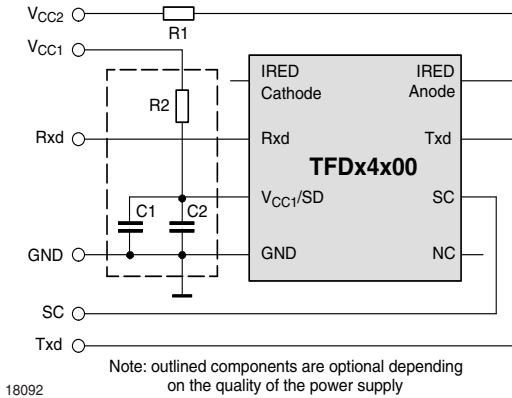


Figure 1. Recommended Application Circuit

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 (see figures 2 and 3), e.g. for IrDA compliant operation ( $V_{CC2} = 5\text{ V} \pm 5\%$ ), a current control resistor of  $14\ \Omega$  is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet and the

eye safety limitations given by IEC825.1. R2, C1 and C2 are optional and dependent on the quality of the supply voltage  $V_{CC1}$  and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

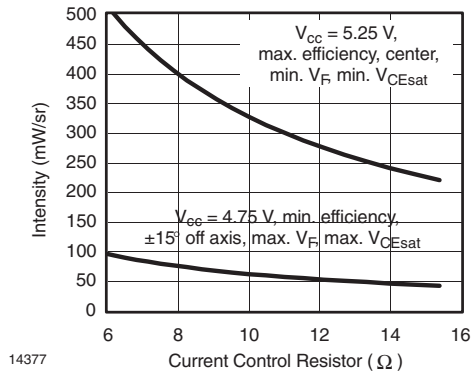


Figure 2.  $I_e$  vs. R1

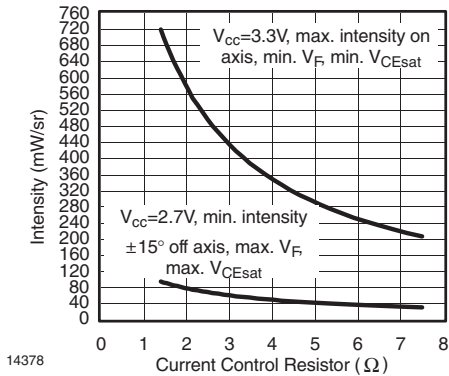


Figure 3.  $I_e$  vs. R1

**Table 1.**  
**Recommended Application Circuit Components**

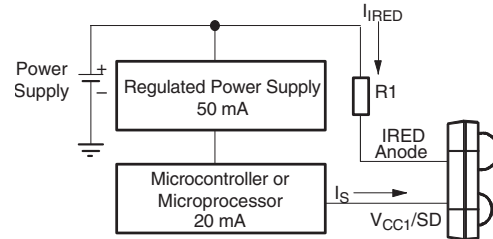
Component	Recommended Value	Vishay Part Number
C1	4.7 $\mu\text{F}$ , Tantalum	293D 475X9 016B 2T
C2	0.1 $\mu\text{F}$ , Ceramic	VJ 1206 Y 104 J XXMT
R1	14 $\Omega$ , 0.25 W (recommended using two 7 $\Omega\text{M}$ , 0.125 W resistor in series, ( $V_{CC2} = 5\text{ V}$ ))	CRCW-1206-7R00-F-RT1
R2	47 $\Omega$ , 0.125 W	CRCW-1206-47R0-F-RT1

The sensitivity control (SC) pin allows the minimum detection irradiance threshold of the transceiver to be lowered when set to a logic HIGH. Lowering the irradiance threshold increases the sensitivity to infrared signals and increases transmission range up to 3 meters. However, setting the Pin SC to logic HIGH also makes the transceiver more susceptible to transmission errors due to an increased sensitivity to fluorescent light disturbances. It is recommended to set the Pin SC to logic LOW or left open if the increased range is not required or if the system will be operating in bright ambient light.

### Shutdown

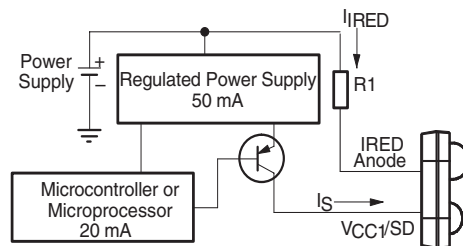
The internal switch for the IRED in Vishay Semiconductors SIR transceivers is designed to be operated like an open collector driver. Thus, the  $V_{CC2}$  source can be an unregulated power supply while only a well regulated power source with a supply current of 1.3 mA connected to  $V_{CC1/SD}$  is needed to provide power to the remainder of the transceiver circuitry in receive mode. The term  $V_{CC1/SD}$  is used here for the power supply pin to indicate that  $V_{CC1}$  can be switched off independently to shut down the transceiver. It is allowed to keep the power supply connected to the IRED Anode. In transmit mode, the current at  $V_{CC1}$  is slightly higher (approximately 4 mA average at 3 V supply current) and the voltage is not required to be kept as stable as in receive mode. A voltage drop of  $V_{CC1}$  is acceptable down to about 2.0 V when buffering the voltage directly from the Pin  $V_{CC1}$  to GND see figure 1). This configuration minimizes the influence of high current surges from the IRED on the internal analog control circuitry of the transceiver and the application circuit. Also board space and cost savings can be achieved by eliminating the additional linear regulator normally needed for the IRED's high current requirements. The transceiver can be very efficiently shutdown by keeping the IRED connected to the power supply  $V_{CC2}$  but switching off  $V_{CC1/SD}$ . The power source to  $V_{CC1/SD}$  can be provided directly from a microcontroller (see figure 4). In shutdown, current loss is realized only as leakage current through the current limiting resistor to the IRED (typically 5 nA). The settling time after switching  $V_{CC1/SD}$  on again is approximately 50  $\mu$ s. Vishay Semiconductors' TOIM4232 interface circuit is designed for this shutdown feature. The  $V_{CC\_SD}$ , S0 or S1 outputs on the TOIM4232 can be used to power the transceiver with the necessary supply current. If the microcontroller or the microprocessor is unable to drive the supply current required by the transceiver, a low-cost SOT23 pnp transistor can be used to switch voltage on and

off from the regulated power supply (see figure 5). The additional component cost is minimal and saves the system designer additional power supply costs.



TFDU4100 (Note: Typical Values Listed)  
 Receive Mode  
 @ 5 V:  $I_{IREd} = 210$  mA,  $I_S = 1.3$  mA  
 @ 2.7 V:  $I_{IREd} = 210$  mA,  $I_S = 1.0$  mA  
 Transmit Mode  
 @ 5 V:  $I_{IREd} = 210$  mA,  $I_S = 5$  mA (Avg.)  
 @ 2.7 V:  $I_{IREd} = 210$  mA,  $I_S = 3.5$  mA (Avg.) 14878

Figure 4.



TFDU4100 (Note: Typical Values Listed)  
 Receive Mode  
 @ 5 V:  $I_{IREd} = 210$  mA,  $I_S = 1.3$  mA  
 @ 2.7 V:  $I_{IREd} = 210$  mA,  $I_S = 1.0$  mA  
 Transmit Mode  
 @ 5 V:  $I_{IREd} = 210$  mA,  $I_S = 5$  mA (Avg.)  
 @ 2.7 V:  $I_{IREd} = 210$  mA,  $I_S = 3.5$  mA (Avg.) 14879

Figure 5.

## Recommended Solder Profiles for TFDU4100

### Solder Profile for Sn/Pb soldering

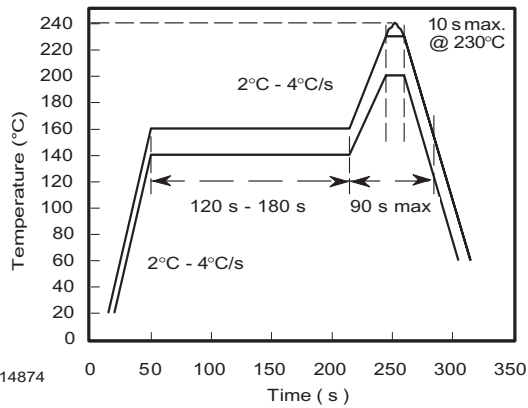


Figure 6. Recommended Solder Profile for Sn/Pb soldering

### Lead Free, Recommended Solder Profile

The TFDU4100 is a lead-free transceiver and qualified for lead-free processing. For lead-free solder paste like  $\text{Sn}_{(3.0 - 4.0)}\text{Ag}_{(0.5 - 0.9)}\text{Cu}$ , there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 7 is Vishay's recommended profile for use with the TFDU4100 transceivers. For more details please refer to Application note: SMD Assembly Instruction.

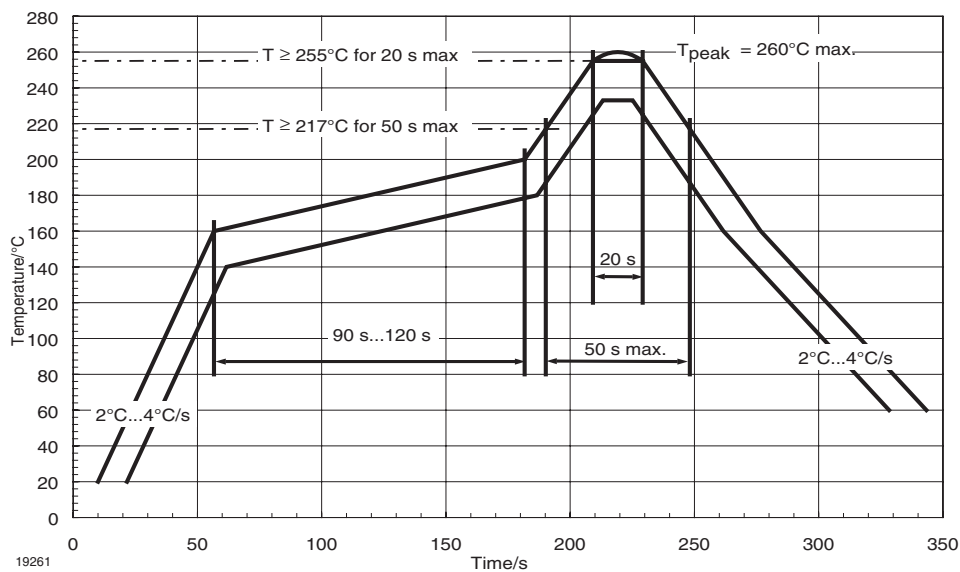


Figure 7. Solder Profile, RSS Recommendation



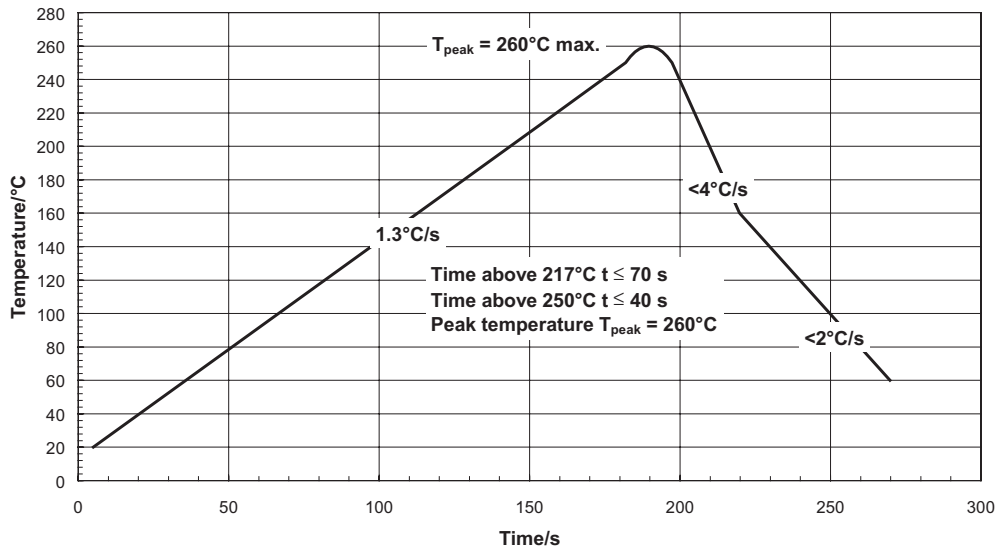


Figure 8. Solder Profile, RTS Recommendation

A ramp-up rate less than 0.9°C/s is not recommended. Ramp-up rates faster than 1.3°C/s damage an optical part because the thermal conductivity is less than compared to a standard IC.

## Current Derating Diagram

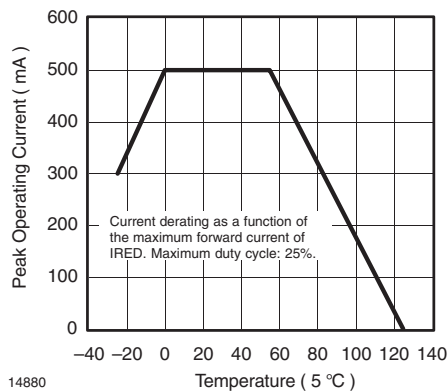
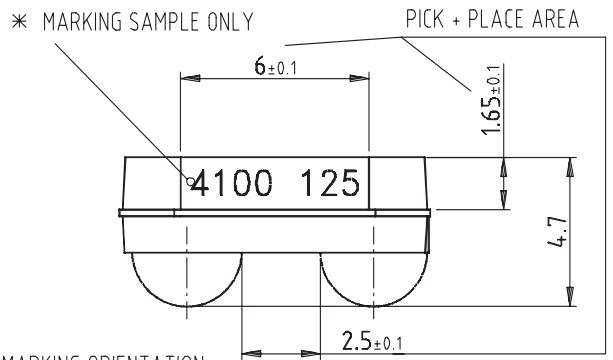
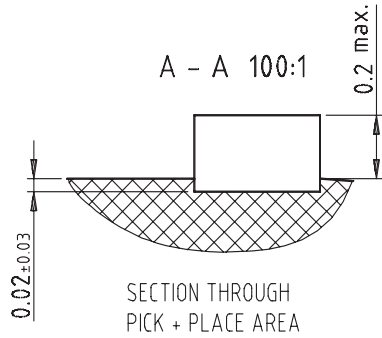
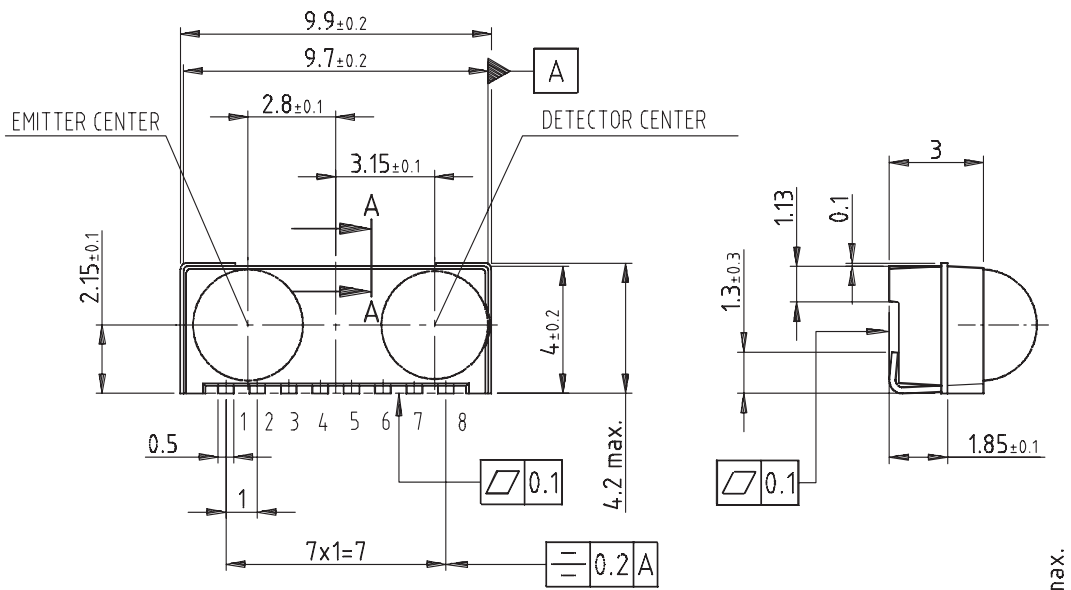
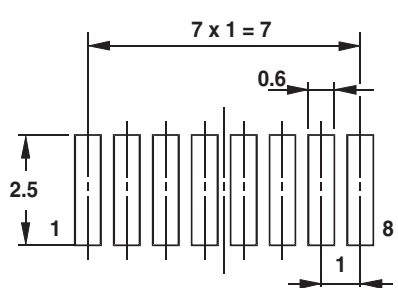
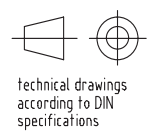


Figure 9. Current Derating Diagram

## Package Dimensions in mm

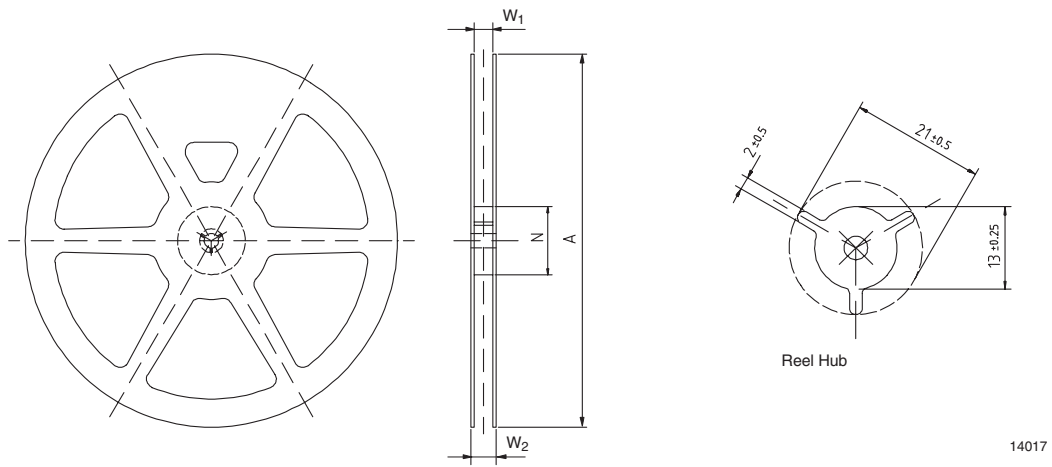


Drawing-No.: 6.550-5148.01-4  
Issue: 11; 29.01.01



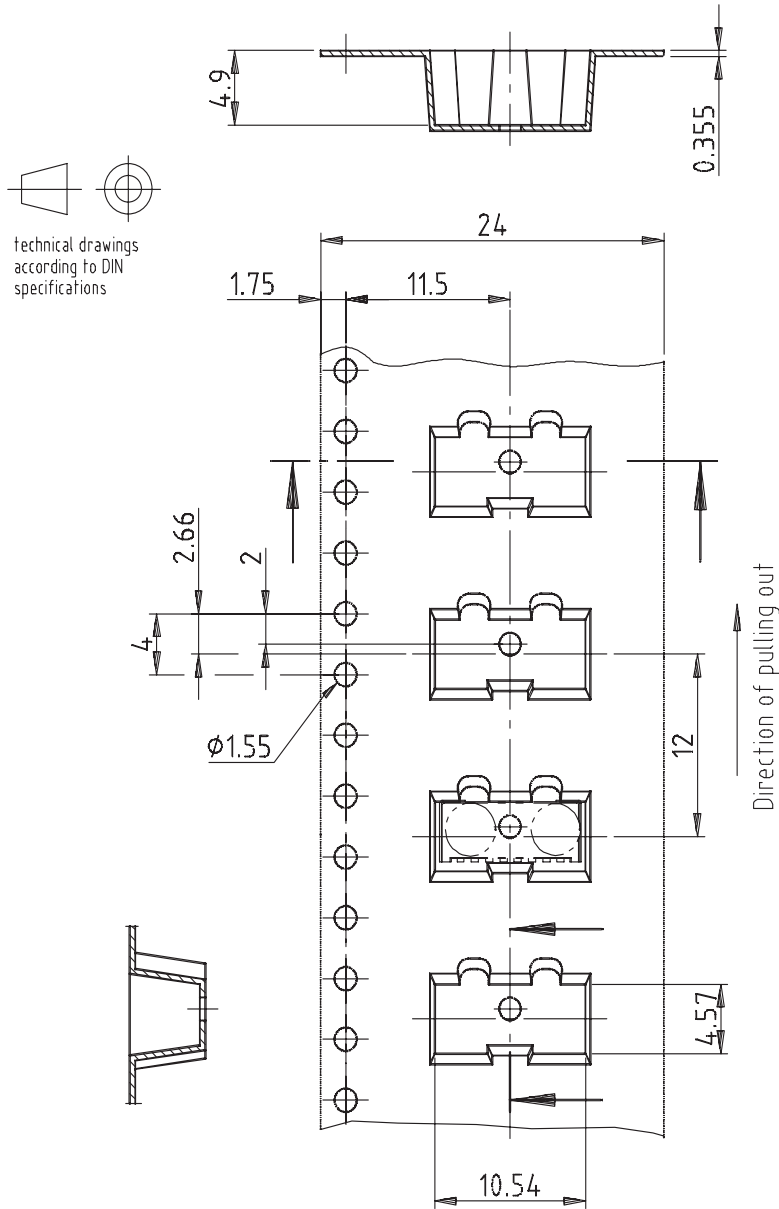
18470

## Reel Dimensions



Tape Width	A max.	N	W <sub>1</sub> min.	W <sub>2</sub> max.	W <sub>3</sub> min.	W <sub>3</sub> max.
mm	mm	mm	mm	mm	mm	mm
24	330	60	24.4	30.4	23.9	27.4

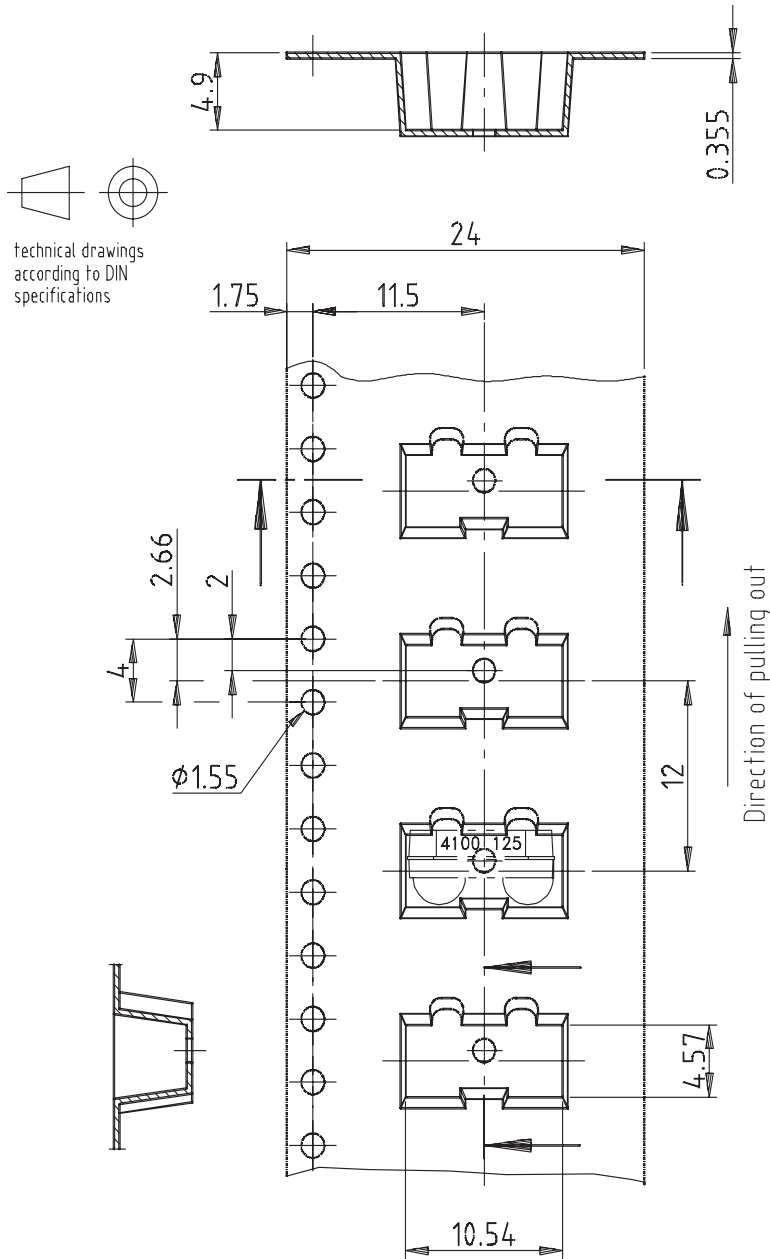
### Tape Dimensions in mm



Drawing-No.: 9.700-5251.01-4

Issue: 2; 07.05.01

18269



Drawing-No.: 9.700-5251.01-4

Issue: 2; 07.05.01

18283

### Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design  
and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany  
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423