| Parameter | Symbol | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| Enable Cycle Time | $t_{CYC}$ | Fig.1, 2 | 500 | – | ns |
| Enable Pulse Width | $PW_{EH}$ | Fig.1, 2 | 230 | – | ns |
| Enable Rise/Fall Time | $t_{Er}$, $t_{Ef}$ | Fig.1, 2 | – | 20 | ns |
| Address Setup Time | $t_{AS}$ | Fig.1, 2 | 40 | – | ns |
| Address Hold Time | $t_{AH}$ | Fig.1, 2 | 10 | – | ns |
| Write Data Setup Time | $t_{DSW}$ | Fig.1 | 80 | – | ns |
| Write Data Hold Time | $t_{DHW}$ | Fig.1 | 10 | – | ns |
| Read Data Delay Time | $t_{DDR}$ | Fig.2 | – | 160 | ns |
| Read Data Hold Time | $t_{DHR}$ | Fig.2 | 5 | – | ns |

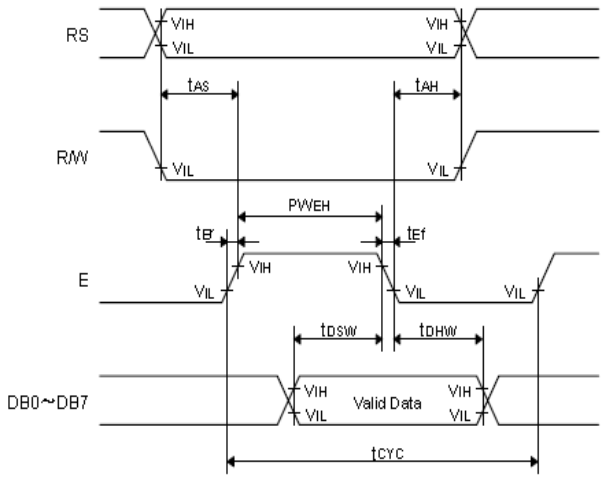


Fig.1 Write Operation Timing



10.3 CPU bus write timing (Parallel interface M68 type)